forming layers of oxide of different thicknesses on the substrate;

forming a common source region for each pair of memory cells;

selectively forming a first layer of polysilicon;

selectively removing the first layer of polysilicon from the common source region;

forming an intermediate dielectric layer; and

forming a second layer of polysilicon to form a common control gate region for pairs of the memory cells having a common source region.

9. A method according to Claim 8 wherein the pairs of memory cells having the common source region belong to a same byte.

10. A method according to Claim 9 wherein the common control gate regions of the pairs of memory cells belonging to the same byte are connected to a common control gate line.

11. A method according to Claim 10 further comprising forming an enabling transistor to address the common control gate line.

12. A method according to Claim 11 wherein the enabling transistor comprises a MOS transistor.

13. A method according to Claim 8 wherein the common control gate region overlies the common source region.

14. A method according to Claim 8 wherein the memory cells-of each pair of memory cells are arranged symmetrically with respect to the common source region.

15. A method for manufacturing a pair of memory cells for an EEPROM including a matrix memory cells, the method comprising:

forming active areas in a substrate for each memory cell;

forming respective drain regions in the substrate for each memory cell;

forming layers of oxide of different thicknesses adjacent the substrate;

forming a common source region in the substrate for the pair of memory cells;

selectively forming a first layer of polysilicon over the substrate;

selectively removing a portion of the first layer of polysilicon from the common source region;

forming an intermediate dielectric layer over the first layer of polysilicon; and

forming a second layer of polysilicon over the intermediate dielectric layer to form a common control gate region for the pair of memory cells.

16. A method according to Claim 15 wherein the common control gate region overlies the common source region.

17. A method according to Claim 15 wherein the memory cells of each pair of memory cells are arranged symmetrically with respect to the common source region.

18. A method of making a memory circuit comprising:

forming a plurality of rows and columns of EEPROM memory cells, each memory cell including a MOS floating gate transistor and a selection transistor; and

symmetrically arranging the memory cells in pairs with a common source region and a common control gate region.

19. A method according to Claim 18 wherein each row of memory cells comprises a word line and each column of memory cells comprises a bit line organized in line groups to group the memory cells in bytes, each of which has an associated control gate line.

20. A method according to Claim 19 wherein the pairs of memory cells having the common source region belong to a same byte.

21. A method according to Claim 20 wherein the common control gate regions of the pairs of memory cells belonging to the same byte are connected to a common control gate line.

22. A method according to Claim 21 further comprising the step of forming an enabling transistor to address the common control gate line.